Active Gate Driving With Full 6-Bit Resolution for Different SiC MOSFETs Using Variable Gate Current Range Digital Gate Driver IC

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***Abstract*-- To eliminate the need to redesign digital gate driver (DGD) ICs for each of a wide variety of power devices, the variable gate current (I_G) range DGD (VIR-DGD) IC with full 6-bit resolution over all ranges was proposed and demonstrated to work in IGBTs [10]. The innovation of VIR-DGD ICs was that a variable resistor on PCB allows one-bit I_G (I_{1BIT}) to be freely varied to achieve the full 6-bit resolution over all ranges for a wide variety of power devices. In this paper, VIR-DGD IC with variable maximum I_G from 0.44 A to 4.4 A and I_{1BIT} from 7.0 mA to 70 mA is applied to SiC MOSFETs for the first time. The trade-off problems between loss and noise during the turn-on switching in two types of SiC modules with 2.6 times different rated current have been successfully solved by an active gate driving using the same VIR-DGD IC.**

***Index Terms*-- Gate driver, switching loss, switching noise, SiC.**

I. Introduction

Digital gate drivers (DGD) ICs, which digitally change the gate current (I_G) multiple times in fine time slots during the switching period of power devices, are attracting attention as a technology that can solve the trade-off problem between loss and noise during power device switching [1-10]. In all conventional DGD ICs [1-9], the I_G range and resolution are fixed for each IC. Different power devices require different I_G ranges and resolutions, which means that DGD ICs must be redesigned for each power device, which has been one of the challenges for the practical application of DGD ICs. For example, in a 6-bit DGD IC, when more than half of the maximum I_G is not needed, the most significant bit is not used, and the IC operates as a 5-bit DGD, thereby preventing DGD from fully utilizing the original 6-bit I_G controllability. Generalizing this, when the maximum I_G required by the user is x times ($0 < x < 1$) the maximum I_G of the DGD ICs, then $\log_2 (1/x)$ bits are unused and wasted. To solve the problem, the variable I_G range DGD (VIR-DGD) IC was proposed in [10]. In [10], the trade-off problems between loss and noise during the turn-on switching in two types of IGBT modules with twice the rated current have been successfully solved by an active gate driving using the same VIR-DGD IC. In this paper, this VIR-DGD IC is applied to SiC MOSFETs for the first time. Specifically, by using the same VIR-DGD IC, the trade-off problems between loss and noise during the turn-on switching in two types of SiC modules with 2.6 times different rated current have been successfully solved.

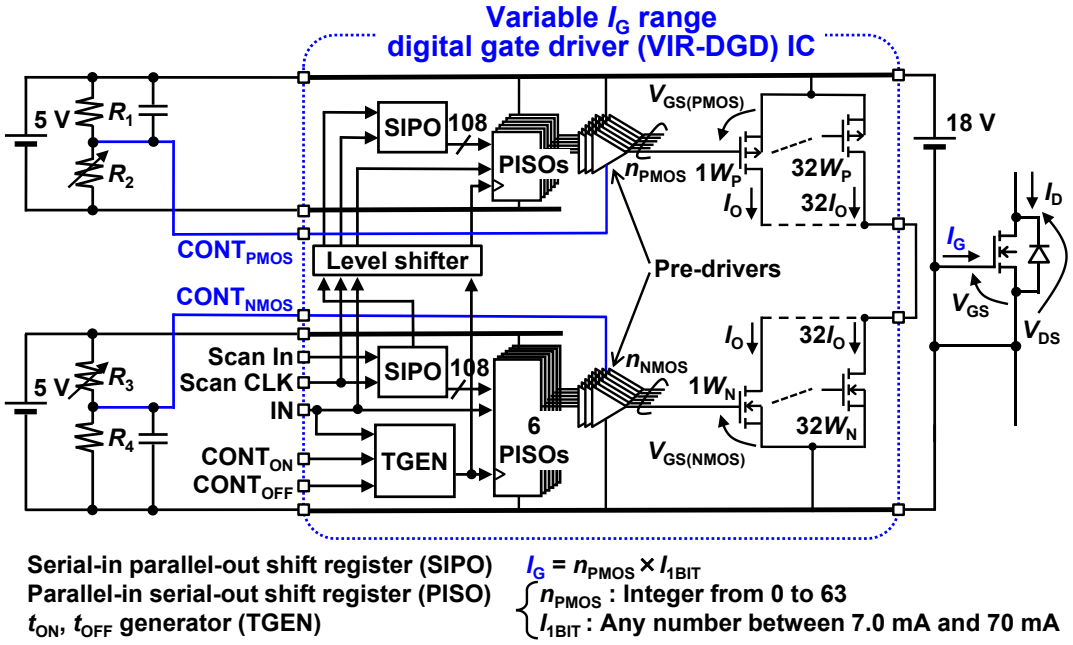


Fig. 1. Circuit schematic of variable I_G range DGD (VIR-DGD) IC [10].

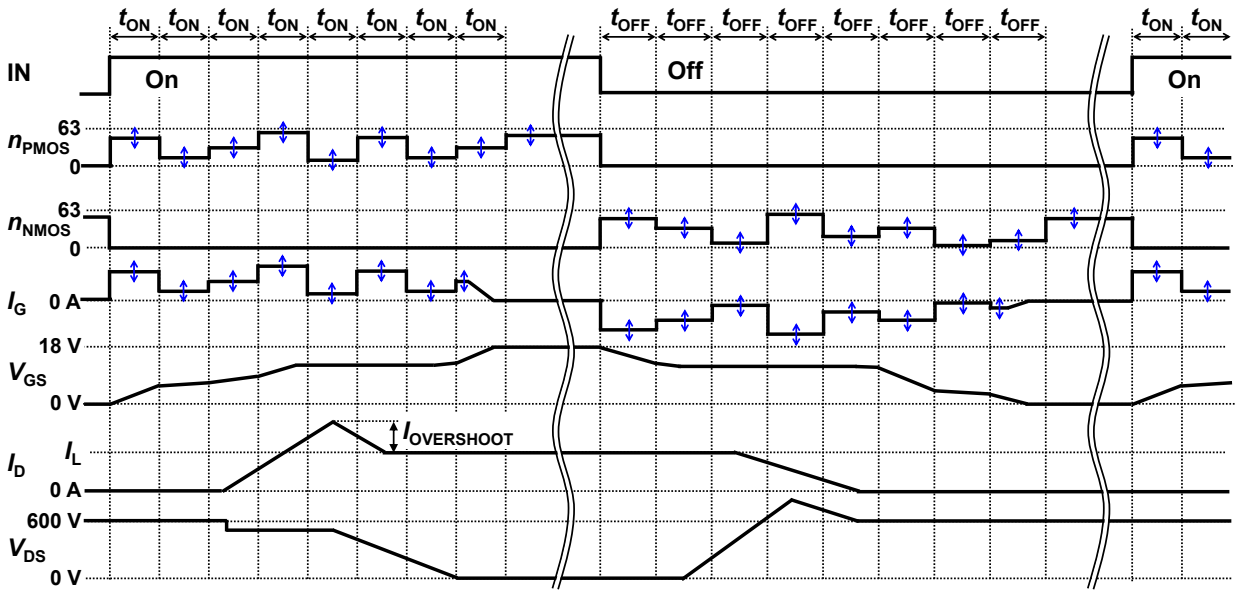


Fig. 2. Timing chart of VIR-DGD IC [10].

II. Variable Gate Current Range Digital Gate Driver IC

Figs. 1 and 2 show a circuit schematic and a timing chart of VIR-DGD IC [10], respectively. In the following, turn-on is discussed for simplicity, whereas the exact same is true for turn-off. In [10], the gate driver output was – 15 V to 15 V to drive IGBTs, while in this paper the gate driver output is 0 V to 18 V to drive SiC MOSFETs. In VIR-DGD IC, $V_{GS\ (PMOS)}$ amplitude of the 6-bit pMOSFETs in the output stage is changed with the analog voltage ($CONT_{PMOS}$) via a variable resistor (R_2) on PCB to realize a variable I_G function. VIR-DGD IC has a t_{ON}, t_{OFF} generator (TGEN), which generates the timing signal that define the time slots (t_{ON}) of the DGD using on-chip voltage controlled oscillators. Though not shown in Fig. 1, t_{ON} can be changed by varying the analog voltage ($CONT_{ON}$) via a variable resistor on PCB. The equation for I_G is shown in Fig. 1. The innovation of the VIR-DGD IC was that it can always achieve 6-bit controllability for a wide variety of power devices, because the 1-bit I_G (I_{1BIT}) is variable by changing $V_{GS\ (PMOS)}$ amplitude [10]. As shown in Fig. 2, I_G can be changed 9 times with 6 bits (= 64 levels) in a t_{ON} time slot. Fig. 3 shows a die photo of VIR-DGD IC [10] fabricated with 180-nm BCD process. The die size is 2.0 mm by 2.5 mm.

III. Measured Results

Fig. 4 shows the measured n_{PMOS} dependence of I_G at four different I_{1BIT} values from 7.0 mA (minimum value) to 70 mA (maximum value), where n_{PMOS} is a 6-bit control bit of I_G and is an integer from 0 to 63. Fig. 4 shows the full 6-bit resolution of I_G over all ranges from 0.44 A to 4.4 A.

Figs. 5 and 6 show a circuit schematic and a measurement setup of the double pulse test using the developed VIR-DGD IC and an SiC module at 600 V, respectively. To demonstrate the broad applicability of the VIR-DGD IC, the same VIR-DGD IC with varied I_{1BIT} is applied to two types of SiC modules (SiC1 and SiC2) with 2.6 times different rated current, as shown in the table in Fig. 5.

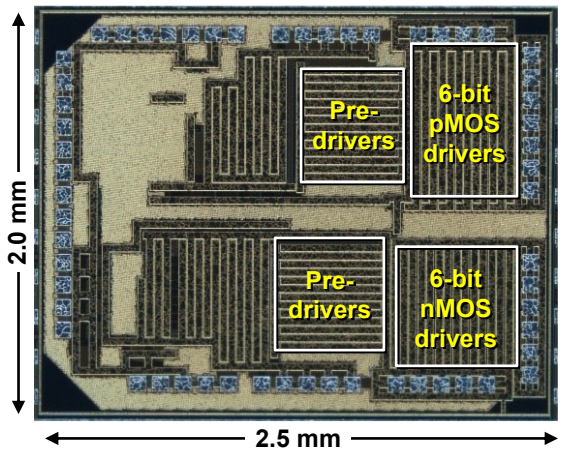


Fig. 3. Die photo of VIR-DGD IC [10].

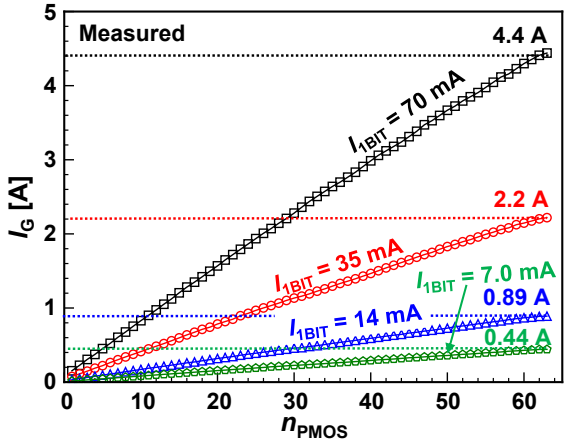
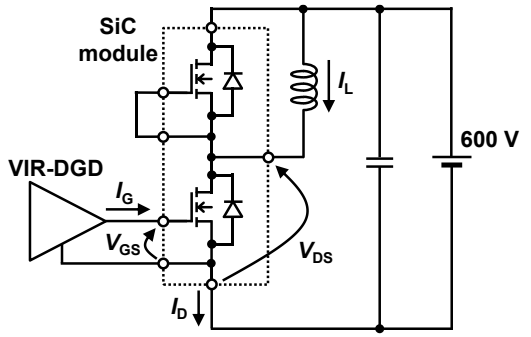


Fig. 4. Measured n_{PMOS} dependence of I_G at four I_{1BIT} values.



Name	Model number	Rating	I_L	I_{1BIT}
SiC1	BSM180D12P2C101	1200 V, 204 A	70 A	35 mA
SiC2	BSM080D12P2C008	1200 V, 80 A	28 A	14 mA

Fig. 5. Circuit schematic of double pulse test. Two types of SiC modules (SiC1 and SiC2) with 2.6 times different rated current are used.

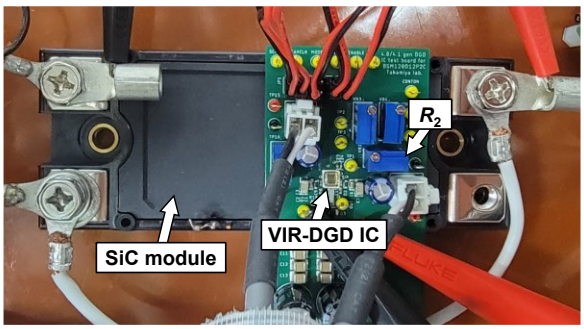


Fig. 6. Measurement setup of double pulse test.

Figs. 7 (a) and (b) show timing charts of the conventional single-step gate driving (SGD) and the proposed active gate driving (AGD) at turn-on for comparison, respectively. In SGD, n is varied, which emulates a conventional gate driver with varied gate resistance. In AGD with 50 ns × 4 slots and a last long slot, four parameters (n_1 to n_4) are varied. Note that [10] used AGD with 140 ns × 4 slots to drive IGBTs, while this paper uses AGD with 50 ns × 4 slots to drive SiC MOSFETs, which switch faster than IGBTs. t_{ON} can be changed from 140 ns to 50 ns by varying the analog voltage ($CONT_{ON}$) via the variable resistor on PCB.

Figs. 8 (a) and (b) show the measured switching loss (E_{LOSS}) vs. drain current overshoot ($I_{OVERSHOOT}$) of the conventional SGD and the proposed AGD in SiC1 (load current (I_L) = 70 A, I_{1BIT} = 35 mA) and SiC2 (I_L = 28 A, I_{1BIT} = 14 mA) at turn-on, respectively. The black curves show the trade-off curves for SGD with varying n. In this paper, an evaluation function (f_{OBJ}) shown in Eq. (1) [1-2, 9] is defined as a performance index of gate driving, and it is discussed that a gate driving with small f_{OBJ} is an excellent gate driving with small E_{LOSS} and $I_{OVERSHOOT}$.

$$f_{OBJ} = \sqrt{\left(\frac{E_{LOSS}}{E_{LOSS,\,MAX}}\right)^2 + \left(\frac{I_{OVERSHOOT}}{I_{OVERSHOOT,\,MAX}}\right)^2}, \qquad (1)$$

where the subscript MAX signifies the maximum of the corresponding quantity. The dotted concentric curves in Fig. 8 show the contour of f_{OBJ}. In the proposed AGD, the

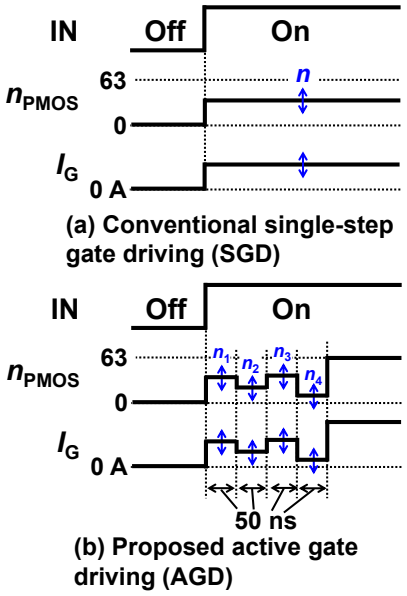


Fig. 7. Timing charts at turn-on. (a) Conventional single-step gate driving (SGD). (b) Proposed active gate driving (AGD).

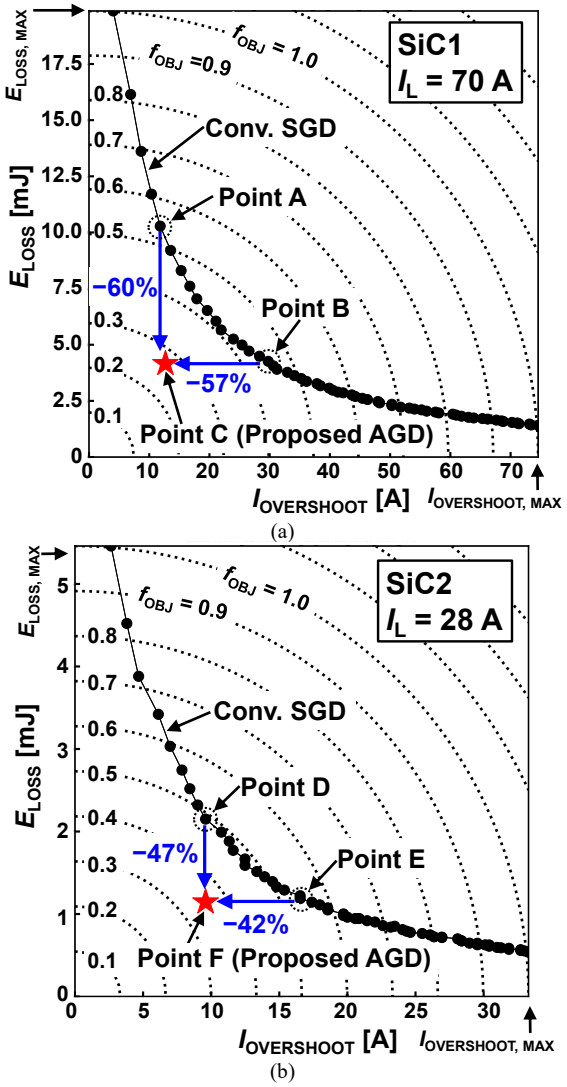
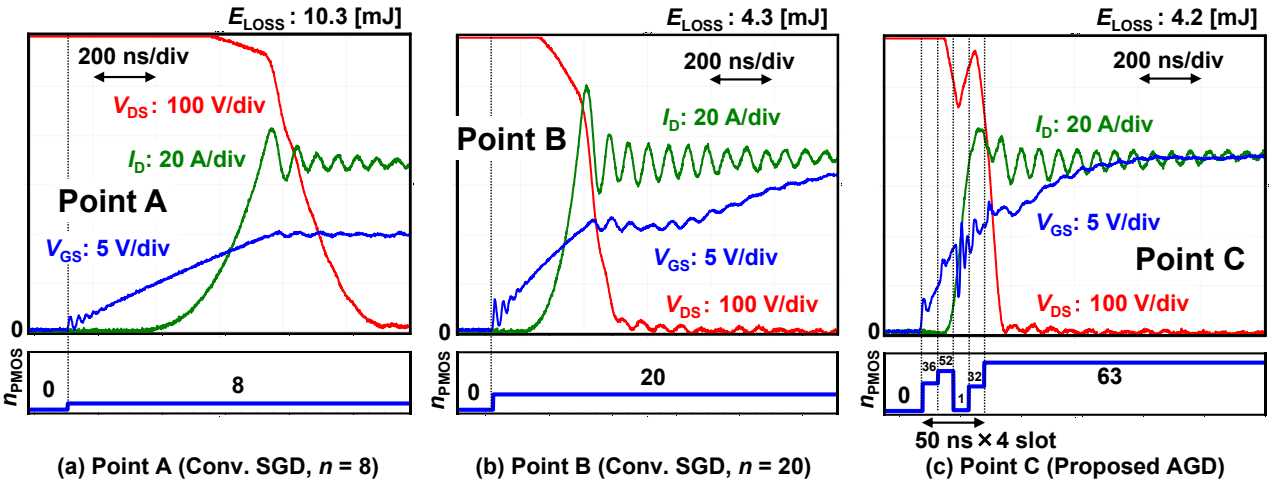
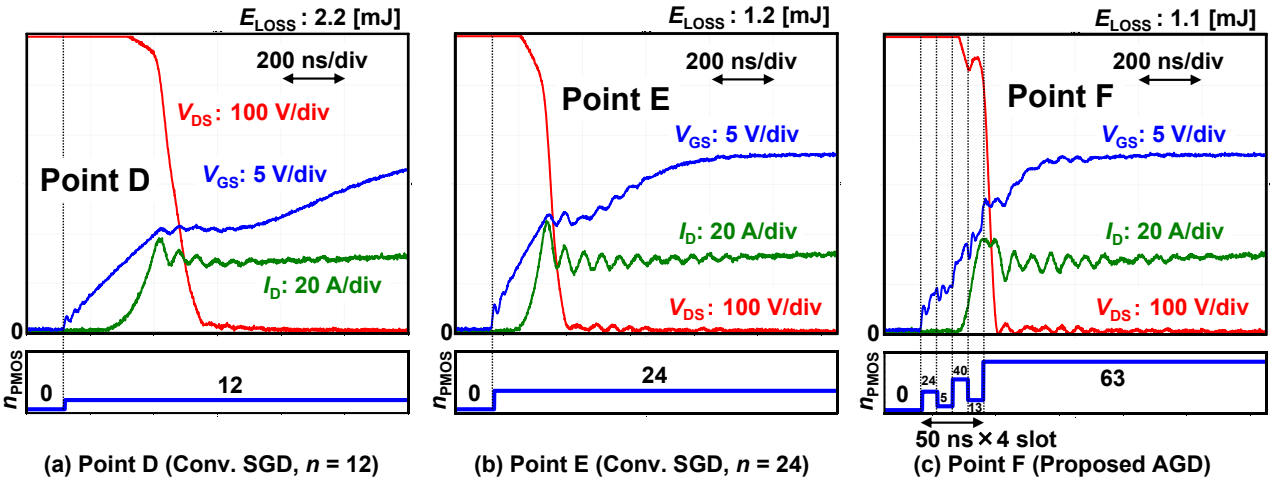


Fig. 8. Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SGD and proposed AGD. (a) SiC1 (204 A rating, I_L = 70 A, I_{1BIT} = 35 mA). (b) SiC2 (80 A rating, I_L = 28 A, I_{1BIT} = 14 mA).



(a) Point A (Conv. SGD, n = 8) (b) Point B (Conv. SGD, n = 20) (c) Point C (Proposed AGD)

Fig. 9. Measured waveforms of Points A to C in Fig. 8 (a).



(a) Point D (Conv. SGD, n = 12) (b) Point E (Conv. SGD, n = 24) (c) Point F (Proposed AGD)

Fig. 10. Measured waveforms of Points D to F in Fig. 8 (b).

TABLE I. COMPARISON TABLE OF DGD ICS

	TPEL'21 [4]	TPEL'21 [3]	ECCE'22 [5]	TPEL'23 [8]	APEC'24 [10]	This work
Target power device	GaN FET	GaN FET	SiC MOSFET	SiC MOSFET	Si IGBT	SiC MOSFET
Process	180 nm BCD	180 nm HV CMOS	180 nm BCD	500 nm HV CMOS	180 nm BCD	180 nm BCD
Max output voltage swing	4.8 V	5 V	30 V	18 V	30 V	18 V
I_G change per switching	8	104	3	30	9	9
Levels of I_G	7 bit	8 bit (coarse), 6 bit (fine)	6 bit	3 bit	6 bit	6 bit
I_G range	Fixed	Fixed	Fixed	Fixed	Variable	Variable
Max I_G	4.8 V / 1.1 Ω = 4.4 A	5 V / 0.12 Ω = 42 A	22 A	3.6 A	0.51–5.1 A	0.44–4.4 A
1 bit of I_G (I_{1BIT})	35 mA	2.6 mA	340 mA	510 mA	8.1-81 mA	7.0-70 mA

double pulse tests are repeated more than 2500 times, and each time E_{LOSS} and $I_{OVERSHOOT}$ are measured to calculate f_{OBJ} defined in Eq. (1), and the combination of the four parameters (n_1 to n_4) that minimizes f_{OBJ} is searched using the simulated annealing algorithm [1]. In Fig. 8 (a), Point C is the best point with the smallest f_{OBJ}. Points A and B are the conventional SGD points with $I_{OVERSHOOT}$ and E_{LOSS} approximately the same as the proposed Point C, respectively. Similarly, in Fig. 8 (b), Point F is the best point with the smallest f_{OBJ}. Points D and E are the conventional SGD points with $I_{OVERSHOOT}$ and E_{LOSS} approximately the same as the proposed Point F, respectively. In SiC1 and SiC2, compared with the conventional SGD, the proposed AGD using the same VIR-DGD IC reduces E_{LOSS} by 60 % and 47 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 57 % and 42 % under E_{LOSS}-aligned condition, respectively.

Fig. 9 shows measured waveforms of Points A to C in Fig. 8 (a). In Fig. 9 (c), the proposed AGD (Point C) achieves low E_{LOSS} and $I_{OVERSHOOT}$ by setting n_{PMOS} to 1 just before the timing of $I_{OVERSHOOT}$. Fig. 10 shows measured waveforms of Points D to F in Fig. 8 (b). In Fig.

10 (c), the proposed AGD (Point F) achieves low E_{LOSS} and $I_{OVERSHOOT}$ by setting n_{PMOS} to 13 just before the timing of $I_{OVERSHOOT}$.

Table I shows a comparison table of DGD ICs. In this paper, VIR-DGD IC [10] demonstrated in IGBTs is applied to SiC MOSFETs for the first time. In conclusion, [10] and this paper demonstrate that the same VIR-DGD IC can properly perform the digital active gate driving for two types of IGBTs (1200 V, 100 A rating and 1200 V, 50 A rating) and two types of SiC MOSFETs (1200 V, 204 A rating and 1200 V, 80 A rating) with full 6-bit resolution, which proves the broad applicability of the proposed VIR-DGD IC.

IV. Conclusions

VIR-DGD IC, which can always achieve 6-bit I_G controllability for a wide variety of power devices, is applied to SiC MOSFETs for the first time. To demonstrate the broad applicability of the VIR-DGD IC, the same VIR-DGD IC with varied I_{1BIT} is applied to two types of SiC modules including SiC1 (204 A rating, I_L = 70 A, I_{1BIT} = 35 mA) and SiC2 (80 A rating, I_L = 28 A, I_{1BIT} = 14 mA). In the turn-on measurements of SiC1 and SiC2 at 600 V, compared with the conventional SGD, the proposed AGD using the same VIR-DGD IC reduces E_{LOSS} by 60 % and 47 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 57 % and 42 % under E_{LOSS}-aligned condition, respectively.

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